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Printed Indium Gallium Zinc Oxide Transistors. Self-Assembled Nanodielectric Effects on Low-Temperature Combustion Growth and Carrier Mobility

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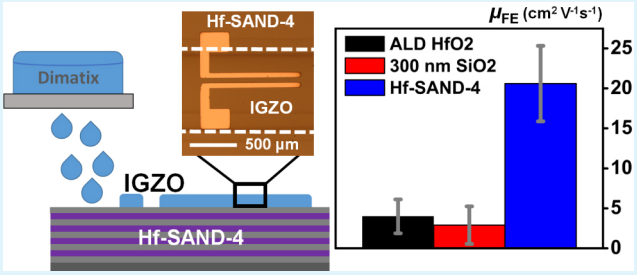
Supporting Information

ABSTRACT: Solution-processed amorphous oxide semiconductors (AOSs) are emerging as important electronic materials for displays and transparent electronics. We report here on the fabrication, microstructure, and performance characteristics of inkjet-printed, low-temperature combustion-processed, amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) grown on solution-processed hafnia self-assembled nanodielectrics (Hf-SANDs). TFT performance for devices processed below 300 °C includes >4× enhancement in electron mobility (μ_{FE}) on Hf-SAND versus SiO_2 or ALD-HfO_2 gate dielectrics, while other metrics such as subthreshold swing (SS), current on:off ratio (I_{ON}:I_{OFF}), threshold voltage (V_{th}), and gate leakage current (I_g) are unchanged or enhanced. Thus, low voltage IGZO/SAND TFT operation (<2 V) is possible with I_{ON}:I_{OFF} = 10^7, SS = 125 mV/dec, near-zero V_{th}, and large electron mobility, μ_{FE}(avg) = 20.6 ± 4.3 cm^2 V^{-1} s^{-1}, μ_{FE}(max) = 50 cm^2 V^{-1} s^{-1}. Furthermore, X-ray diffraction analysis indicates that the 300 °C IGZO combustion processing leaves the underlying Hf-SAND microstructure and capacitance intact. This work establishes the compatibility and advantages of all-solution, low-temperature fabrication of inkjet-printed, combustion-derived high-mobility IGZO TFTs integrated with self-assembled hybrid organic−inorganic nanodielectrics.



KEYWORDS: *hybrid dielectric, inkjet-printing, amorphous oxide field-effect transistor, low-voltage electronics, electron mobility, thin-film transistor*

INTRODUCTION

Inorganic amorphous oxide semiconductors (AOSs) such as indium gallium zinc oxide (IGZO) are poised for widespread commercial application in liquid crystal display (LCD) thin-film transistor (TFT) backplane circuitry as a replacement for hydrogenated amorphous silicon.[1−5] To date, AOSs offer attractive physical and electronic properties versus other unconventional electronic materials such as organic small molecules and polymers, or nanomaterials.[1,2,6−10] AOS properties such as large electron mobilities, good device stability and lifetime, solution-processability, optical transparency, mechanical flexibility, and relatively simple syntheses are hallmarks of these materials.[1,2,6,7,11−19] Therefore, significant research efforts have focused on investigating, understanding, and optimizing AOSs for technology insertion.[1,2,20−26] Note that although many AOS applications (e.g., LCD backplanes) currently rely on capital-intensive vacuum sputter deposition of the semiconductor layer, additive solution-based printing techniques offer the possibility of producing electronics at higher throughput as well as with reduced cost and waste.[3−5,12,27−31] Nevertheless, current-generation solution-processing technologies (e.g., sol−gel) are not optimal because of the high required temperatures, which are incompatible with typical flexible polymer substrates, and the presence of extraneous solvents, precursor counterions and/or organic ligands which may remain as performance-degrading contaminants.[13−15,27,32] Thus, for AOS solution processing methods, extensive research has focused on reducing film growth/densification temperatures, on developing compatible patterning methods, and on enhancing TFT metrics such as electron mobility (μ_{FE}), subthreshold swing (SS), current on:off ratio (I_{ON}:I_{OFF}), threshold voltage (V_{th}), and gate leakage current (I_g).

With regard to materials strategies to enhance TFT performance and power efficiency, incorporating higher capacitance gate dielectrics (C_i, eq 1) and maximizing the field-effect mobility (μ_{FE}, eq 2) are of great importance.[33] This combination will ensure higher drive currents (I_{ds}) at lower operating voltages (V_g, V_{th}), for a given device architecture, and is essential for low-power portable applications such as RF-ID tags, sensors, integrated logic circuits, and consumer electronics

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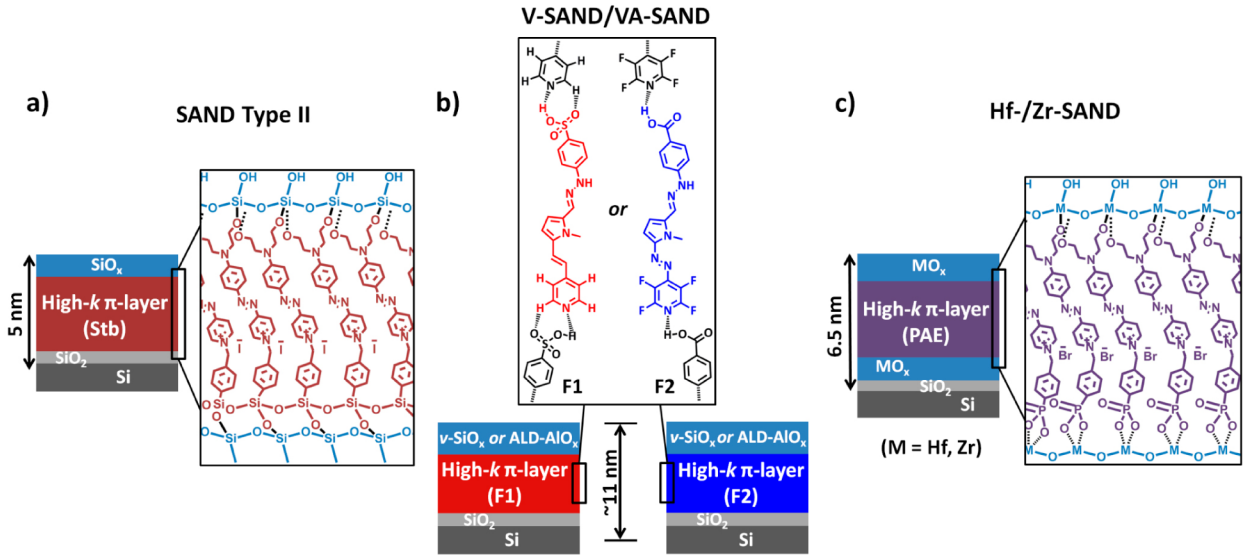

Figure 1. Self-assembled nanodielectric (SAND) gate dielectric structures. (a) Halosilane-derived Type II SAND;[43]. (b) Vapor-deposited V-SAND/VA-SAND.[44,45] (c) Zirconia/hafnia-phosphonate-derived Zr-/Hf-SAND.[46,47] PAE = 4-[[4-[bis(2-hydroxyethyl)-amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl]pyridinium bromide.

applications such as computers, tablets, and cellular telephone displays. Recent reports on IGZO transistors have focused on substrate and gate dielectric materials, including those offering some degree of mechanical flexibility and optical transparency.[1,7,14,18,34] However, little work has incorporated inkjet printing.

$$C_i = \frac{C}{A} = \frac{\varepsilon_0 k}{d} \quad (1)$$

$$I_{ds} = \left(\frac{W}{2L}\right) C_i \mu_{FE} (V_g - V_{th})^2 \quad (2)$$

A notable exception is a 2009 report that describes inkjet-printed IGZO films on SiO_2 annealed at 450 °C that showed a mobility of ~0.03 $cm^2\ V^{-1}\ s^{-1}$.[1,30] Other metrics for these devices were I_{ON}:I_{OFF} = 10^4, on current = 0.1 mA, V_{th} = 6.2 V, and subthreshold swing (SS) = 1500 mV/dec over a V_{ds} range of 5−10 V.[1,30] Although this work was an advance for oxide inkjet printing, these metrics are not competitive with a-Si:H technologies that provide $\mu_e \approx 1\ cm^2\ V^{-1}\ s^{-1}$.[2] In the same year, inkjet printing was reported to produce high-performance zinc indium tin oxide (ZITO; closely related to IGZO) TFTs with field-effect mobilities near 30 $cm^2\ V^{-1}\ s^{-1}$, I_{ON}:I_{OFF} = 10^5, V_{th} = 2.0 V, and I_{ds} ~ 1 mA.[28] However, the channel width: length ratio (W:L) used was only 7:1, less than the preferred 20:1 used in the present study, and known to yield mobilities overestimated by 2× or more.[35] Furthermore, the best gate (V_g) and source−drain bias (V_{ds}) voltages exceeded 40 V because of the low capacitance dielectric used, and 600 °C annealing was required to obtain the reported TFT performance.[28] Such processing temperatures are incompatible with flexible or disposable substrates such as plastics,[36,37] and lower temperatures did not afford useful device performance.[28]

Recently, a "sol−gel on-chip" approach was used for indium zinc oxide (IZO) and IGZO transistors, resulting in devices with μ_{FE} as high as 10 $cm^2\ V^{-1}\ s^{-1}$ and 5 $cm^2\ V^{-1}\ s^{-1}$, respectively, using solution-based spin-coating and relatively mild annealing temperatures (≤275 °C).[38] Device reproducibility/uniformity was excellent, and threshold voltages were centered near 0 V. Nevertheless, TFT fabrication in this case first requires the synthesis of an elaborate organometallic precursor for each metal ion, and this process has not yet been used with inkjet-printing. A 2012 report explored alternative routes to low-temperature sol−gel densification using deep-UV radiation (λ = 254 and 185 nm) to produce IGZO, IZO, and In_2O_3 TFTs with mobilities up to 14 $cm^2\ V^{-1}\ s^{-1}$ on an alumina gate dielectric.[39] TFT performance metrics included SS = 97 mV/dec, I_{ON}:I_{OFF} = 10^6, μ_{avg} ~9 $cm^2\ V^{-1}\ s^{-1}$, I_{ds} = 0.1 mA, and V_{th} = 2.7 V at V_{ds} = 5−10 V. Substrate temperatures reached ~160 °C during UV exposure, which was later reported to be essential for these metrics. Indeed, comparable TFT performance could also be achieved with 350 °C thermal-only processing.

We recently reported a fundamentally different, low-temperature "combustion chemistry" approach to AOS sol−gel processing.[14] This technique utilizes local, intrafilm exothermic processes to densify AOS thin films in situ, thereby significantly reducing the external heat required for TFT-quality films. Using acetylacetone as the fuel and metal nitrate salts as oxidizers, films of In_2O_3, IZO, and zinc tin oxide (ZTO) were efficiently prepared. In_2O_3 TFTs with large μ_{FE} values of 13 $cm^2\ V^{-1}\ s^{-1}$ were achieved, with more complex oxides, including ZTO and IZO, exhibiting comparable TFT metrics. Thermal analysis of the combustion process indicates abrupt and essentially complete mass loss/densification at far lower temperatures than possible by conventional sol−gel processes (e.g., at 200−300 °C vs 500−600 °C).[1] Note that using solution-processed amorphous-alumina as the gate dielectric rather than 300 nm SiO_2 increases the In_2O_3 electron mobility from 1 $cm^2\ V^{-1}\ s^{-1}$ to 13 $cm^2\ V^{-1}\ s^{-1}$ for 200 °C processing, and from 3.3 $cm^2\ V^{-1}\ s^{-1}$ to nearly 40 $cm^2\ V^{-1}\ s^{-1}$ for 250 °C processing of the spin-coated thin films. The increased mobility is primarily attributable to lower interface trap densities at the amorphous-alumina dielectric-semiconductor interface, estimated from subthreshold swing data.[14] Shortly thereafter, it was reported that inkjet-printed, conventionally processed sol−gel IGZO films had mobilities of 2.5 $cm^2\ V^{-1}\ s^{-1}$ in a bottom S-D

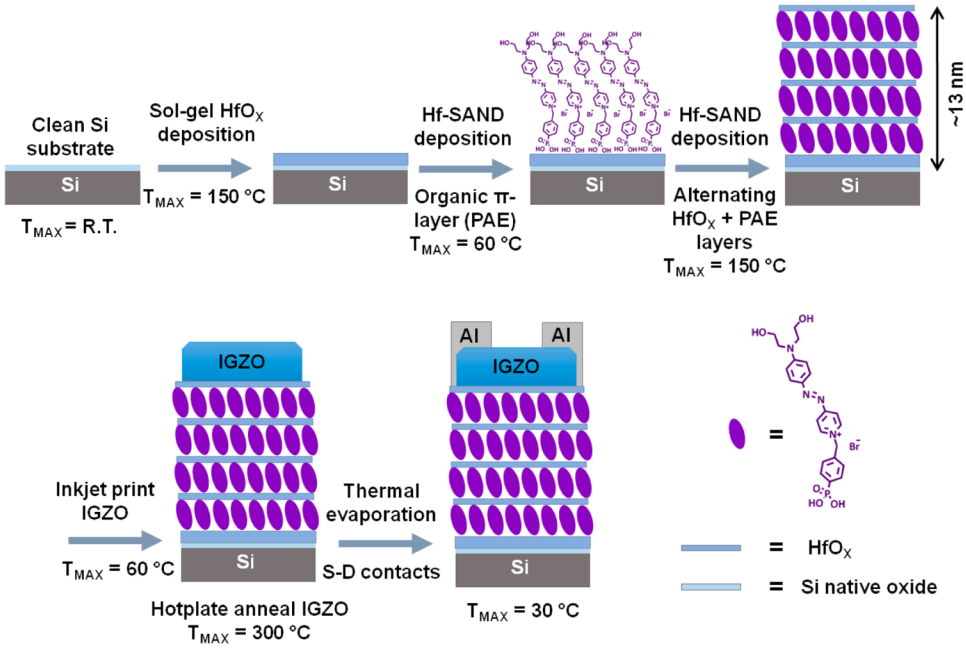

Figure 2. Amorphous IGZO TFT deposition protocol with maximum process temperatures denoted at each step (components not to scale).

contact configuration with a SiO_2 gate dielectric, setting a performance benchmark for printed IGZO TFTs at the time.[12]

The dramatically increased AOS mobility enabled by the aforementioned amorphous-alumina gate dielectric exemplifies the need to better understand and optimize dielectric-semiconductor interfaces. The rapid emergence of unconventional semiconductor and dielectric materials over the past decade[1,2,8,9,33,40−42] presents opportunities for dielectric-semiconductor interfacial control. For example, we have developed a series of self-assembled nanodielectrics (SANDs) that are customized for hydrocarbon solution growth (Figure 1a),[43] vapor phase growth (Figure 1b),[44,45] or solution growth under ambient conditions[46,47] (Figure 1c).

Each class offers modular tunability, high capacitance, low leakage currents, structural regularity, smooth surfaces, good environmental/thermal stability, radiation hardness, and facile integration with diverse organic, inorganic, and nanomaterial semiconductors.[33,41−43,45−52] In general, these materials significantly enhance TFT metrics such as mobility and suppress trapped charge.[42,52−54] The impressive properties raise the intriguing question of whether combining SANDs with combustion AOS processing is possible, in view of the temperatures involved, whether the SAND microstructure, high capacitance, and low leakage currents are preserved under these conditions, and whether high-performance TFTs can be realized via all solution-processing.

It will be seen here that combining inkjet-printed, 300 °C combustion processed a-IGZO films with a multilayer Hf-SAND[47] gate dielectric affords average saturation field-effect mobilities (μ_{FE}(avg)) of 20.6 ± 4.3 $cm^2\ V^{-1}\ s^{-1}$, with some devices achieving mobilities as high as 50 $cm^2\ V^{-1}\ s^{-1}$. In contrast, comparably processed a-IGZO devices fabricated on SiO_2 or ALD-HfO_x gate dielectrics exhibit μ_{FE}(avg) = 2.9 ± 2.1 $cm^2\ V^{-1}\ s^{-1}$ and 4.0 ± 2.4 $cm^2\ V^{-1}\ s^{-1}$, respectively.[12−14,27,32] These results illustrate that Hf-SAND-gated devices retain dielectric integrity under AOS combustion processing conditions and provide electron mobilities nearly 10x greater than possible with inkjet-printed conventionally processed IGZO sol−gel thin films.[12] In addition, the inkjet-printed combustion IGZO TFTs simultaneously attain competitive transistor performance benchmarks such as low voltage (<2 V) operation, I_{ON}:I_{OFF} = 10^7, excellent subthreshold swing = 125 mV/dec, and near zero V_{th}.

RESULTS AND DISCUSSION

In the following sections, we first discuss the SAND dielectric and ALD-HfO_x processing strategies and the properties of the resulting materials. A detailed discussion of TFT fabrication follows including examination of the microstructural and electronic properties. Finally, we summarize significant results, and provide suggestions for future exploration.

Dielectric Fabrication. The layer-by-layer deposition of Hf-SAND (Figure 2) begins by first cutting and solvent cleaning a heavily doped native oxide Si wafer inside a Class 10 HEPA filtered clean hood to avoid particle contamination. After activating the substrate surface with an air plasma, four alternating layers of self-assembled organic π-layer (PAE)[46] and HfO_x are grown from solution to obtain the final Hf-SAND-4 coated substrates.[47] The control HfO_x gate dielectric was grown by 170 ALD cycles at 150 °C (similar to the maximum process temperature of the Hf-SAND) using a $Hf(NMe_2)_4$ precursor and affords a calibrated growth rate of ~0.9 Å/cycle. The dielectric thickness was 15.8 ± 0.3 nm as obtained by ellipsometry. After the Hf-SAND and HfO_x deposition, all three dielectrics (SiO_2, HfO_x, Hf-SAND) were processed in parallel for the remaining steps of the IGZO transistor fabrication.

a-IGZO TFT Fabrication. Individual 0.0125 M combustion sol−gel precursors, which are derived from metal nitrate salts ($In(NO_3)_3{\cdot}xH_2O$; $Zn(NO_3)_2{\cdot}6H_2O$; $Ga(NO_3)_3{\cdot}xH_2O$), are mixed and stirred (see Experimental Section), aged overnight, and then combined in a 72.5:7.5:20 atom % ratio (In:Ga:Zn) ~2 h before inkjet printing. This a-IGZO composition was chosen to achieve maximum mobility while maintaining stable and reproducible I_{ON}:I_{OFF} and V_{th}.[27,32] Under these synthetic conditions, the IGZO films are amorphous by XRD and

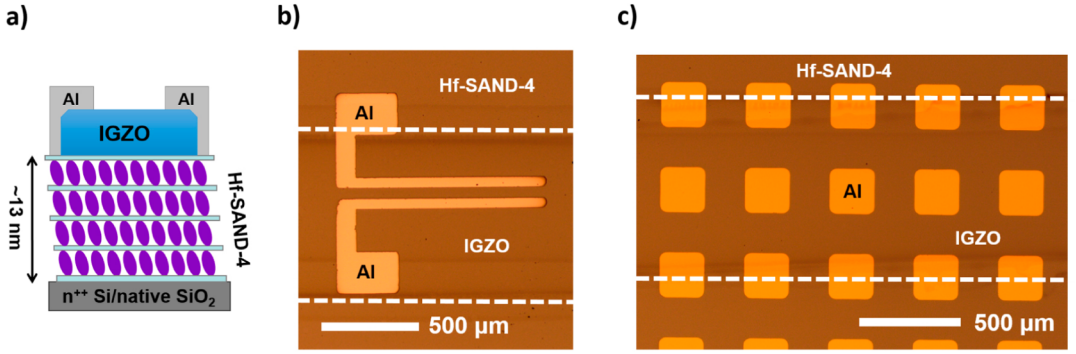

Figure 3. (a) Cross-section schematic of the combustion a-IGZO/Hf-SAND device structure examined in this study (components not to scale); (b) optical micrograph of a completed inkjet-printed a-IGZO transistor on Hf-SAND (white dashed line denotes approximate boundary of the printed a-IGZO line); (c) capacitor array near the a-IGZO line used for extraction of the dielectric capacitance (white dashed line denotes approximate boundary of printed a-IGZO line).

Table 1. IGZO TFT Device Parameters As a Function of Dielectric Type, Averaged over Five Devices in Each Category

dielectric	d (nm)	C_i (nF/cm^2)	V_{DS} (V)	μ_{FE} (cm^2/(V s))	I_{ON} (mA)	I_{ON}:I_{OFF}	V_{th} (V)	SS (mV/dec)	g_m[a] (μS)
SiO_2/Si	300	11	100	3	3.7	7×10^6	14	4700	40
ALD HfO_2	16	590	1	4	0.13	2×10^6	0.4	200	50
Hf-SAND-4	13	605[b]	1	20	0.67	1.3×10^7	0.0	190	300

[a] $g_m = dI_{ds}/dV_g$. [b] 635 nF/cm^2 upper estimate from XRR-derived cross-section profiles.

selected area electron diffraction.[27] After briefly activating the dielectric surface with an air plasma, rectangular patterns of IGZO were printed with a Dimatix materials printer and processed at 300 °C for 20 min. A total of 5 layers were printed in regular succession, with the final IGZO layer annealed at 300 °C in a humidity controlled box at 45% R.H. The maximum process temperature for the entire fabrication was 300 °C, and the process flow with corresponding maximum process temperatures at each step is depicted in Figure 2. Representative device cross-sections and optical micrographs of devices reported in this study are shown in Figure 3. Finally, a series of devices were measured for each dielectric type and used to extract the average electrical properties detailed in Table 1.

Electrical Properties of Inkjet Printed IGZO Transistors. To evaluate the device metrics of the a-IGZO/Hf-SAND TFTs, a-IGZO/SiO_2 devices were initially fabricated as controls. The dramatic differences in device performance observed versus Hf-SAND motivated including ALD-HfO_x as a secondary control since the capacitance approximates that of Hf-SAND (see the Supporting Information, Figure S1). Table 1 summarizes relevant device performance metrics including field-effect mobility (μ_{FE}), subthreshold swing (SS), transconductance (g_m), on state S-D current (I_{ds}), current on:off ratio (I_{ON}:I_{OFF}), dielectric capacitance (C_i), and threshold voltage (V_{th}). As depicted in the overlay transfer plot of three different a-IGZO TFTs in Figure 4a, the Hf-SAND-gated TFT outperforms the others by a significant margin, with equivalent on state I_{ds} as the SiO_2 control and nearly 8× the I_{ds} of ALD-HfO_x. This results in calculated electron mobilities (eq 3)[13] ~4× larger than on SiO_2, and more than double those of ALD-HfO_x as compared to the Hf-SAND-4/a-IGZO devices.

$$\mu_{FE} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{ds}}}{\partial V_g}\right) \quad (3)$$

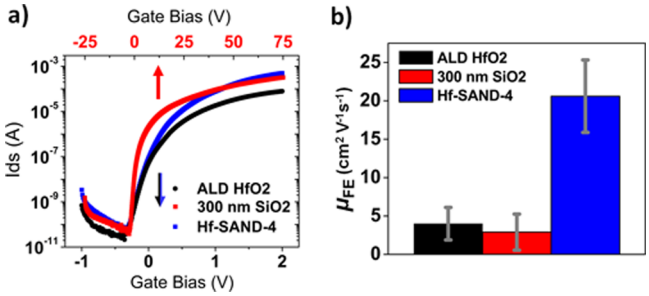

Figure 4. (a) Semi-log transfer plot overlay of inkjet-printed IGZO transistors on the three dielectrics examined in this study; (b) average field-effect electron mobilities of the devices constructed during this study as a function of dielectric type.

The I_{ds} differences between the HfO_x and Hf-SAND gated TFTs are observed even though the capacitances (C_i) are dissimilar. The ALD-HfO_x exhibits an areal C_i of ~590 nF/cm^2, whereas the multilayer Hf-SAND-4 C_i is ~605 ± 30 nF/cm^2 (see Figure S1a in the Supporting Information). This offers the possibility of driving the TFTs at similar gate fields and voltage biasing conditions, eliminating additional variables that may affect the a-IGZO transport properties. The frequency dependent capacitance response of Hf-SAND can be found in the Supporting Information (Figure S3).

Subthreshold swing metrics appear to be substantially enhanced when moving to the thinner, higher capacitance dielectric materials (vs C_i = 11 nF/cm^2 for 300 nm SiO_2). In fact, both ALD-HfO_x and Hf-SAND-4 gated TFTs exhibit comparable average SS (eq 4) of ~200 mV/dec, which is near the literature benchmark values for IGZO.[1,2] Several "champion" Hf-SAND devices exhibit SS ~125 mV/dec, which is impressive for the low-temperature solution processing utilized. This likely reflects low levels of interface traps in the

$$SS = \frac{\partial V_g}{\partial \log I_{ds}} \quad (4)$$

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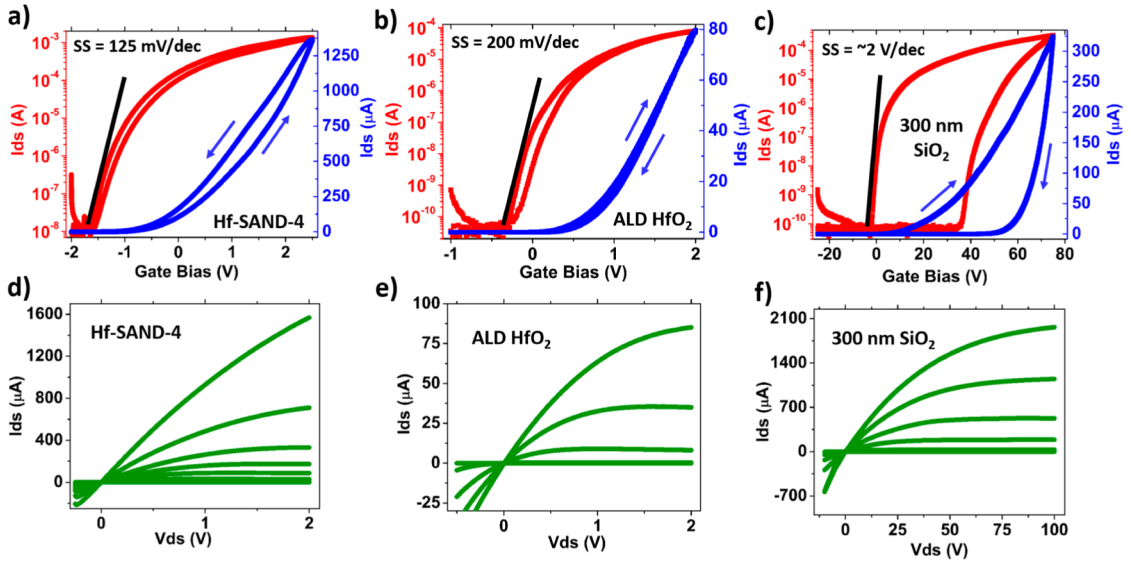

Figure 5. Semi-log transfer and linear output plots for representative a-IGZO transistors and their subthreshold swing (SS) metrics as a function of indicated dielectric material; (a ,d) Hf-SAND, (b, e) ALD-grown HfO_2, (c, f) 300 nm SiO_2/Si wafers.

thinner Hf-SAND layers in addition to the increased capacitance.[2,17,55] The SS also decreases more than an order of magnitude versus the SiO_2 control, which is on average greater than 4 V/dec. Note also that the operating voltage of the devices has decreased by nearly 2 orders of magnitude on Hf-SAND and ALD-HfO_x versus SiO_2 (Figures 4a and 5). The integration of IGZO with Hf-SAND therefore enables device operation at only 2 V while still maintaining an I_{ds} value of greater than 1 mA and near 0 V V_{th}.

Note that I_{ON}:I_{OFF} is also very large for the a-IGZO/Hf-SAND TFT ($\sim 1 \times 10^7$), and shows very little deviation from the controls (average I_{ON}:I_{OFF} = 4.5×10^6). It is remarkable that the I_{ON}:I_{OFF} is not severely gate leakage current limited even though the dielectric is processed entirely from solution (at 150 °C maximum process T), is ~13 nm thick, and that the devices are large (TFT channel L x W = 50 × 1000 μm, Figure 3b). Gate leakage (I_g) is typically <10 nA even at the extremes of the biasing window (V_g = 2 V, see Figure S2 in the Supporting Information). Although I_{ON}:I_{OFF} is indeed large for all devices in this study, the Hf-SAND-gated devices maintain large I_{ds} with high mobility as well, which should be sufficient to drive active matrix display pixels, logic-based/integrated circuit networks, or other post-Si electronic technologies.[1,2] The average I_{ON} for the a-IGZO/Hf-SAND devices is just under 1 mA (Table 1), although 1−2 mA on currents are possible at sub-2 V operation in many devices (see Figure 5d).

The threshold voltage for the present a-IGZO/Hf-SAND TFTs is also essentially zero, whereas the ALD-HfO_x TFTs have a slightly positive, but still small V_{th} = +0.4 V (Table 1). As expected because of interface traps and the large operating voltages necessary for the SiO_2-gated TFTs, V_{th} = +14 V.[2] This V_{th} on SiO_2 is also near the value for well-optimized a-IGZO/SiO_2 TFTs.[27] The near-zero V_{th} on Hf-SAND, indicating low levels of dielectric fixed charge and bulk trap states,[2,17,55] along with sub-2 V operation, further reinforce the possibility of producing very low-power, high-performance devices with a-IGZO/Hf-SAND.[2,17,56−61] Next, the microstructural and morphological properties of the a-IGZO/Hf-SAND devices are examined to better understand the device performance.

Physical Properties of Inkjet-Printed IGZO Transistors. AFM is first used to the study the morphology of the printed a-IGZO thin films and the underlying dielectric. X-ray reflectivity (XRR) analysis is then used to probe the nanostructure of the underlying Hf-SAND multilayer before and after the combustion process, as well as the properties of the printed a-IGZO. Finally, X-ray photoelectron spectroscopy (XPS) is used to extract a-IGZO chemical composition in a completed device.

AFM Characterization. In Figure 6, AFM scans of the annealed, inkjet-printed a-IGZO on Hf-SAND-4 (a, b) and on 300 nm SiO_2 (c, d) are shown. There is little detectable difference between the images for the large area and small area scans, with no evidence of microstructure or grain boundaries. a-IGZO rms roughness values are ~2 Å for the Hf-SAND-4 and SiO_2 substrates, indicating well-formed continuous films,

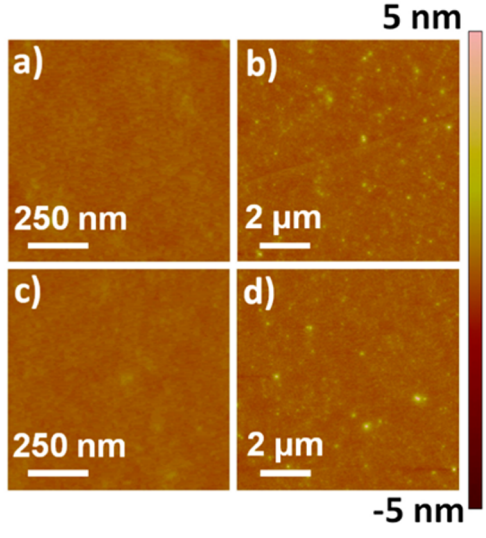

Figure 6. (a) 1 × 1 μm and (b) 10 × 10 μm tapping mode AFM scans of inkjet printed a-IGZO on Hf-SAND-4; (c) 1 × 1 μm and (d) 10 × 10 μm tapping mode AFM scans of inkjet printed a-IGZO on 300 nm SiO_2.

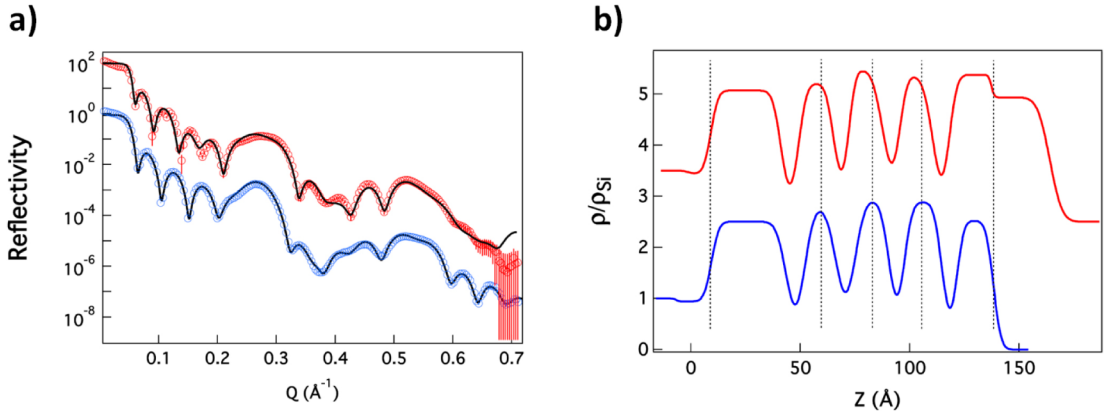

Figure 7. (a) X-ray reflectivity (XRR) of a-IGZO-coated Hf-SAND-4 (red) and Hf-SAND-4 only (blue) substrates produced in this study. Best-fit results are shown in black; (b) Corresponding electron density profiles normalized to the bulk Si density of the device structures obtained by XRR, (red) a-IGZO-coated Hf-SAND-4, (blue) Hf-SAND only. Substrates are ⟨100⟩ polished Si.

consistent with earlier reports that combustion-processed AOS films are smooth and conformal.[12−15,32] AFM scans of the uncoated dielectrics also reveal very smooth surfaces, with ALD-HfO_x exhibiting an rms roughness of ∼2.6 Å (see Figure S3 in the Supporting Information) and Hf-SAND-4 having an rms roughness of 1.3 Å.[47] The slightly rougher ALD-HfO_x could conceivably affect the measured a-IGZO mobility given that the SiO_2 wafer roughness is typically ∼2 Å.[62]

XRR Characterization. X-ray reflectivity is an excellent tool to probe nanostructural order and electron density within semiconducting or insulating thin-films, especially SANDs.[45−47,63−66] In the present case, XRR measurements are critical to understanding any nanostructural changes occurring in Hf-SAND-4 as a result of the combustion processing, since significant changes could in principle affect thickness, capacitance, and the extracted electron mobility from eq 3. Underestimating the capacitance would result in overestimating the carrier mobility values. The Hf-SAND capacitance was measured as near to the printed a-IGZO line as possible (≤500 μm lateral distance, Figure 2c and Figure S1b in the Supporting Information) to minimize other artifacts that affect capacitance.

In earlier work, the dielectric properties and nanostructures of analogous zirconium oxide dielectrics (Zr-SANDs) were examined before and after high temperature annealing.[46,67] The initial SAND thickness decreases from ∼115 Å to ∼100 Å after 400 °C exposure for 30 min--roughly 13% of the total starting thickness. In contrast, XRR analysis[67] of combustion-processed a-IGZO/SAND TFTs shown in Figure 7 indicates only very slight shifts in the Hf-SAND structural features (indicated by the vertical dashed gray lines in Figure 7b) on printing and combustion processing the overlying a-IGZO layer at 300 °C for 20 min. Although the measured overall thickness is unchanged, as evidenced by the rightmost dashed gray line, some of the interior layers appear to shift by ∼5 Å. Assuming that the maximum total contraction of the four-layer dielectric is on this order (notwithstanding the data provided by the aforementioned gray line), and that the initial Hf-SAND-4 thickness is 130 Å as given by the blue curve in Figure 7b, this suggests the SAND under the a-IGZO contracts by at most 4% (125 Å/130 Å) of the total initial thickness under the combustion processing. Therefore, using the capacitance measured directly adjacent to the printed a-IGZO line (605 nF/cm^2) as a reference, and modeling an equivalent decrease in thickness, this affords an effective capacitance increase of ∼30 nF/cm^2, yielding a maximum total estimated capacitance of ∼635 nF/cm^2 under the a-IGZO line. Inserting this value into eq 3 yields statistically insignificant differences in the calculated mobility (±5%, ± ∼1 cm^2 V^{-1} s^{-1}), and thus does not impact the nearly 5-fold mobility enhancement observed between the a-IGZO/Hf-SAND-4 and the control dielectrics.

The XRR also offers insight into the properties of the a-IGZO. Although the fabrication protocols require printing five separate a-IGZO layers, no electron density deviations are evident in the rightmost region of the red upper curve in Figure 7b. This indicates a dense, uniform a-IGZO layer with a thickness of 27 Å (see Figure S4b in the Supporting Information), which should allow efficient coupling to the gate electrode.[68] Limited deviations in this thickness are observed between the different dielectrics, as well as the wetting properties of the IGZO precursor solution upon printing, which gives consistent printed line widths (∼800 μm).

A recent publication by Wang et al. examined the effect of IGZO film thickness on TFT device performance.[69] When the IGZO film thickness was varied from 23 to 125 nm, they found that maximum performance occurs at a thickness of 55 nm, while thinner films become more sensitive to dielectric defects (interfacial roughness, charge traps), or atmospheric adsorbents (O_2, CO_2). In the present study, the combustion processed IGZO film thickness was intentionally kept low in order to minimize void formation during combustion gas evolution.[13,14] Although some controversy exists on the precise definition of thin-film combustion,[70] we stress that films derived from dilute precursor solutions are an effective approach to AOS technologies. The work by Wang et. al suggests that one explanation for the enhanced mobility we find with Hf-SAND may be the very thin IGZO films (∼30 Å), and consequently, it is unlikely that small differences in IGZO thickness alone can be reasonably associated with the enhanced transistor performance presented in this study. This further implicates the Hf-SAND as the origin of the exceptional transistor performance. Additional XRR data can be viewed in the Supporting Information (see Figure S5 and Tables S1 and S2). Finally, given that the total Hf-SAND-4 thickness does not vary significantly in a-IGZO processing, it can be concluded that local combustion exothermicity is not severe enough to dramatically degrade the SAND microstructure.

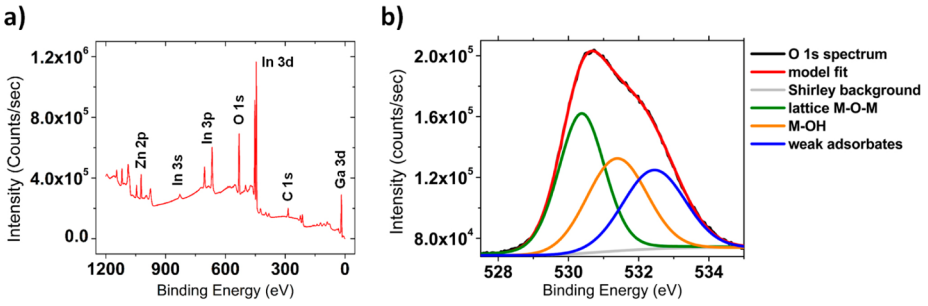

Figure 8. (a) XPS survey scan of a 300 °C inkjet printed combustion-processed a-IGZO line on a Hf-SAND-4 coated Si substrate; (b) high-resolution O 1s XPS scan of inkjet printed IGZO (black) with model fits (color) on the same substrate.

XPS Characterization. Lastly, the chemical composition of the printed, combustion-processed a-IGZO lines were analyzed by XPS. An XPS survey scan is shown in Figure 8. All expected elements are clearly distinguishable (Figure 8a) with no obvious impurities. The high-resolution O 1s scan shown in Figure 8b is useful for assaying the extent of a-IGZO lattice densification.[14,15,27,32] The three subpeaks comprising the spectrum can be identified as: 530.2 ± 0.2 eV, lattice M-O-M bonds (green); 531.2 ± 0.2 eV, bulk and surface metal hydroxides (orange), and 532.2 ± 0.2 eV, weakly bound surface adsorbates such as water or carbon dioxide (blue).[15,27] It is now well-established that AOS TFT charge transport is sensitive not only to the demsotu of M-O-M lattice formation within the film, but also to back channel surface adsorbates (the top a-IGZO-air interface), which is a function of device construction and geometry.[55] The relative O 1s subpeak ratios can be used to qualitatively assess the potential of the material for good TFT performance.[27] The dominant peak at ~530 eV in Figure 8b indicates a densified AOS lattice in the TFT channel region, in contrast to the peak at ~532 eV, which shows contributions from weakly bound back channel adsorbates. Neglecting relative intensity effects due to physical depth from the a-IGZO-air interface, the M-O-M subpeak to O 1s peak area ratio $\eta_{M\text{-}O\text{-}M}$ = 0.40, is within the generally accepted range for good semiconductor performance.[27] Thus, the inkjet-printed, combustion-processed a-IGZO lines produced here are well-densified, and variations in a-IGZO/dielectric performance can reasonably be attributed to differences in the underlying dielectric.

TFT Response as a Function of Gate Dielectric. Although the low SS values for a-IGZO/ALD-HfO_x and a-IGZO/Hf-SAND TFTs benefit from large capacitances and relatively low interface charge trap densities,[2,14] the mobility differences enabled by the two dielectrics reflects currently unresolved issues concerning how a-IGZO transport mechanisms are influenced by the gate dielectric.[1,2,17,61,71−83] The Hf-SAND-4 architecture has four separate π-organic layers by design, to enhance capacitance and minimize pinhole related leakage pathways, and comprises nearly 50% of the SAND thickness. It is possible that the significant organic content acts to offset pinholes between oxide nanolayers while suppressing/negating significant densities of charged oxide impurities at the dielectric-semiconductor interface.[40,43,48] Note that plausible a-IGZO mobility-limiting mechanisms originating in the underlying dielectric include Coulombic scattering because of ionized fixed charges, remote polar phonon scattering, and interfacial roughness.[56,84]

Recent studies have characterized the transport properties of a-IGZO TFTs having plasma-ALD grown TiO_x/SiN_x gate dielectric bilayers.[81] Holding the SiN_x thickness constant at 200 nm while varying the high-k TiO_x thickness at the dielectric-IGZO interface from 2 to 8 nm, reveals that μ_{FE} falls from 9.9 $cm^2\ V^{-1}\ s^{-1}$ (2 nm TiO_x) to 1.8 $cm^2\ V^{-1}\ s^{-1}$ (8 nm TiO_x) as the TiO_x thickness is increased, while for SiN_X-only devices μ_{FE} = 12.5 $cm^2\ V^{-1}\ s^{-1}$.[85] These observations and the mobility temperature dependence as a function of TiO_x thickness implicate Coulomb scattering because of immobile fixed charges in the bulk TiO_x as limiting the a-IGZO μ_{FE}. This mobility degradation occurs while the SS remains constant, similar to the Hf-SAND vs ALD-HfO_x behavior observed in this study, and arguing that trapped interfacial charge remains nearly the same for the two dielectrics. Note that the uppermost layer of Hf-SAND in intimate contact with the a-IGZO channel is ~2 nm of HfO_x as measured by XRR (see Figure S4b in the Supporting Information), analogous to the higher mobility case described above with TiO_X. HfO_2 properties other than fixed-charge Coulombic-scattering sites, such as polar phonons and interfacial roughness, could also affect the a-IGZO transport.[2,10,16,17,46,84,85] However, while differences in interfacial roughness measured by AFM, ALD-HfO_x = ~3 Å vs Hf-SAND = ~1.5 Å, may contribute to carrier scattering because the TFT channel is in close proximity to the dielectric-IGZO interface,[1,2,17,33,68,69] it seems unlikely that the large mobility differences observed here can be attributed solely to interfacial roughness differences.

Further evidence for dielectric-specific a-IGZO scattering processes as observed here is provided by studies of sputter deposited TFTs having either 15 nm HfO_x or bilayer SiO_2/HfO_2 gate dielectrics (SiO_2 in contact with the IGZO). The electron mobility of the former is 5× smaller than the latter (1.4 $cm^2\ V^{-1}\ s^{-1}$ vs 7 $cm^2\ V^{-1}\ s^{-1}$) and was attributed to greater Coulomb scattering in the former.[56] Yet another example is provided by sputtered IGZO TFTs having high-k HfO_2, ZrO_2, Al_2O_3, and Ta_2O_5 dielectrics. It was reported that bulk dielectric trap states, as assayed by $C-V$ hysteresis and V_{th} shifts, depress μ_{FE} and I_{ds} most severely for HfO_2 and Al_2O_3.[86] Taken together, these results argue that the origin of SAND TFT mobility enhancement is related to low densities of Coulombic scattering centers and polar phonons, consistent with the hybrid organic−inorganic architecture,[33,42] and highlighting not only (a) the sensitivity of a-IGZO semiconductor transport to thick high-k oxide dielectric layers at the dielectric-semiconductor interface, which appears to be relatively insensitive to the specific growth technique, but also (b) the attraction of hybrid dielectric materials such as SANDs for maximizing applications-related AOS TFT performance. Combining synergistic advances in solution-based semiconductor and dielectric materials processing therefore affords high-perform-

ance a-IGZO TFTs with device metrics exceeding considerably those reported previously at such low processing temperatures and with inkjet printing.

CONCLUSIONS

Hf-SAND is a promising gate dielectric to enable unconventional semiconducting materials, as illustrated here in combination with inkjet-printed, low-temperature combustion-processed amorphous IGZO. Low voltage IGZO/SAND TFT operation (<2 V) is possible with I_{ON}:I_{OFF} = 10^7, SS = 125 mV/dec, near-zero V_{th}, and large electron mobility, μ_{FE}(avg) = 20.6 ± 4.3 $cm^2\ V^{-1}\ s^{-1}$, μ_{FE}(max) = 50 $cm^2\ V^{-1}\ s^{-1}$. Diffraction analysis indicates that the 300 °C IGZO combustion processing leaves the underlying Hf-SAND microstructure and capacitance essentially unchanged. Importantly, the local exothermicity of the combustion IGZO does not significantly affect the underlying dielectric, which is important for future integration strategies. We suggest that a-IGZO/Hf-SAND-4 is well-suited for display electronics and/or for other emerging transistor technologies where high performance is desired with moderate temperature based solution processing and printing. Overall, this work reveals the attributes of all-solution, low-temperature fabrication of inkjet-printed, combustion-derived high-mobility a-IGZO TFTs integrated with self-assembled hybrid organic–inorganic nanodielectrics.

EXPERIMENTAL SECTION

Hf-SAND Fabrication. Hf-SAND and ALD-HfO_x gate dielectrics utilized commercially available polished Si as substrates (WRS Materials, ⟨100⟩, *n*++, 0–0.018 Ω-cm resistivity), which are cut with wafer dicing tape (Semiconductor Equipment Corporation) to avoid particle contamination, and then ultrasonicated in acetone and isopropanol in a Class 10 HEPA filtered NuAire clean hood. Thermally oxidized Si/300 nm SiO_2 wafers used as controls were obtained from WRS Materials (⟨100⟩, p++, 1–5 Ω-cm resistivity). Immediately prior to spinning of the first HfO_x sol–gel layer or ALD deposition, the substrates were exposed to an air plasma (550 mTorr chamber pressure, "high" power, Harrick PDC-32G) for 150 s to produce a clean, hydrophilic surface. Exposure to ambient was limited to <5 min before either spin-coating or ALD chamber pump down. The sol–gel HfO_x layers were spin-coated (5000 rpm, 30 s, 5015 rpm/s acceleration, Laurell Tech) and immediately placed on a 150 °C preheated hot plate for 40 min. Alternating layers of self-assembled organic π-layer (PAE)[46] and HfO_x were deposited as described elsewhere[47] to obtain Hf-SAND-4 coated substrates. The control HfO_x dielectric layer was grown by ALD (Cambridge NanoTech) using 170 cycles of $Hf(NMe_2)_4$ precursor (Sigma-Aldrich) at 150 °C to yield a calibrated growth rate of ∼0.9 Å/cycle. The 15.8 ± 0.3 nm film thickness was obtained by ellipsometry (J. A. Woollam M-2000). After the Hf-SAND and HfO_x deposition, all three dielectrics (SiO_2, HfO_x, Hf-SAND) were processed in parallel for the remaining steps of the IGZO transistor fabrication.

IGZO TFT Fabrication. Before initiating the transistor fabrication, "combustion"-based sol–gel precursors were formulated by individually dissolving metal nitrate salts (176.1 mg $In(NO_3)_3{\cdot}xH_2O$; 148.6 mg $Zn(NO_3)_2{\cdot}6H_2O$; 198.2 mg $Ga(NO_3)_3{\cdot}xH_2O$) in 10 mL of anhydrous 2-methoxyethanol, followed by the addition of 55 μL of aqueous NH_3 (14.5 M) and 100 μL of acetylacetone under stirring. After the solutions were allowed to age overnight with stirring, the precursors were combined in a 72.5:7.5:20 atom % ratio (In:Ga:Zn) ∼2h before inkjet printing at 0.0125 M solution concentration, which was stirred continuously at room temperature until use. All solutions were filtered through a 0.45 μm PTFE syringe filter (Pall Acrodisc) before introduction into the printer cartridge. TFT fabrication was followed by cleaning/activating the dielectric surface with an air plasma (Harrick PDC-32G, 5 s, "medium" power, 550 mTorr chamber pressure) and placing the substrates onto a preheated (60 °C) Dimatix printer platen (FujiFilm Dimatix DMP-2800). The initial a-IGZO lines (two 8 mm × 2 mm rectangles horizontally separated by 3 mm) were printed on the substrates and immediately placed onto a preheated 300 °C hot plate for 20 min. Subsequent layers (5 total) were printed by removing the substrate from the hot plate and placing directly on the 60 °C printer platen. The alignment procedure (typically 2–3 min) allowed the substrate temperature to equilibrate with the platen before the next IGZO layer was deposited. The final (5th) IGZO layer was similarly annealed at 300 °C, but in a humidity controlled box at 45% R.H.

To ensure good IGZO contact, Al top source-drain (S-D) contacts were deposited by thermal evaporation through a shadow mask immediately upon completion of inkjet printing, with the total time in ambient <1 h. Device substrates were typically held under high vacuum (∼1 × 10^{-6} Torr) for 2 h before contact deposition. After depositing 60 nm Al (∼1 Å/s deposition rate), the devices were removed and stored under N_2 in the dark. Devices were characterized electrically ≤18 h after contact deposition. TFT performance was found to be insensitive to this time interval. Device performance metrics were extracted from first scans of the transistor devices to avoid overestimation of performance via mechanisms related to filling of dielectric traps, hysteresis suppression, etc.[87−89]

To aide in extracting mobility, square Al capacitor pads (200 μm × 200 μm) were deposited concurrently with the S-D contacts (via shadow mask) and then measured in parallel with the transistors to obtain the capacitance as near the IGZO line as possible (≤500 μm lateral distance). Five devices were measured for each dielectric type and the data used to calculate the average electrical properties. Measurements were obtained using a three-point probe station in the dark at ambient temperature and humidity, with a locally written LabView program driving two Keithley 2400 SourceMeter units. Dielectric *C*–*V* measurements were obtained via a Keithley 4200SCS semiconductor parameter analyzer system with a 30 mV input oscillation amplitude (OSC) at 10 kHz frequency.

Atomic Force Microscopy (AFM). All AFM images for surface roughness analysis were collected using a Dimension ICON (Bruker) AFM in air with tapping mode. Probe tips were sourced from AppNano with a tip radius of curvature ≈ 6 nm (ACTA) and spring constant 37 N/m driven at 300 kHz frequency.

X-ray Photoelectron Spectroscopy (XPS). XPS utilized a ThermoFisher ESCALab 250Xi equipped with a monochromated Al Kα X-ray source. An electron flood gun beam energy of 10 eV and an emission current of 0.002 mA were used for charge compensation. Spectra binding energy shifts were normalized relative to C 1s (285.0 eV) prior to peak fitting (XPS PEAK 4.1).

X-ray Reflectivity (XRR). X-ray reflectivity measurements were preformed on an 18 kW Rigaku ATXG diffractometer. X-rays were generated from the Cu rotating anode (X-ray wavelength is λ = 0.1541 nm) and collimated to produce a monochromated beam of dimensions 5.0 mm ×0.1 mm and 1 × 10^8 photons per second flux at the sample surface. The XRR data were modeled and fitted by applying the Abeles matrix method used in the MOTOFIT package[67] to obtain the thickness, electron density, and interfacial roughness information of each layer.

ASSOCIATED CONTENT

Supporting Information

Dielectric capacitance data, device optical micrographs, IGZO/Hf-SAND TFT gate leakage data, ALD-HfO_x AFM roughness data, and additional XRR data. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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